the finished device wafer. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 um. The wide metal lines can, for instance, be of aluminum or electroplated copper. These layers of dielectric and metal lines can be used for power buses or power planes, clock distribution networks, critical signal, re-distribution of I/O pads for flip chip applications, and for long signal paths.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of the interconnection scheme of the present invention.

Fig. 2 shows a cross section of the present invention in a more complex circuit configuration.

Fig. 3a shows the top view of a combination power and X-signal plane using the present invention.

Fig. 3b shows the top view of a combination power and Y-signal plane using the present invention.

Fig. 4 shows the top view of solder bump arrangement using the present invention and is an expanded view of a portion of Fig. 5.

Fig. 5 shows the top view of an example of power/ground pads combined with signal pad using the present invention.

Fig. 6 shows a basic integrated circuit (IC) interconnect scheme of the invention.

Fig. 7 shows an extension of the basic IC interconnect scheme by adding power, ground and signal distribution capabilities.

Fig. 8 shows an approach of how to transition from sub-micron metal to wide metal interconnects.

Fig. 9 shows detail regarding BGA device fan out using the invention.

Fig. 10 shows detail regarding BGA device pad relocation using the invention.

Fig. 11 shows detail regarding the usage of common power, ground and signal pads for BGA devices using the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention teaches an Integrated Circuit structure where key re-distribution and interconnection metal layers and dielectric layers are added over a conventional IC. These re-distribution and interconnection layers allow for wider buses and reduce conventional RC delay.

Referring now more specifically to Fig. 1, there is shown a cross section of one implementation of the present invention. A silicon substrate 1 has transistors and other devices, typically formed of poly silicon, covered by a dielectric layer 2 deposited over the devices and the substrate. Layer 3 indicates the totality of metal layers and dielectric layers that are typically created on top of the device layer 2. Points of contact 6, such as bonding pads known in the semiconductor art, are in the top surface of layers 3 and are part of layer 3. These points of contact 6 are points within the IC arrangement that need to be further connected to surrounding circuitry, that is to power lines or to signal lines. A passivation layer 4, formed of for example silicon nitride, is deposited on top of